WHAT IS CLAIMED IS:

1. An debug and emulation system comprising:

a target device embodied in a single integrated circuit including

an function clock circuit generating an function clock;

an operation circuit connected to said function clock circuit operating in synchronism with said function clock;

a trace trigger circuit connected to said function clock circuit and said operation circuit, said trace trigger circuit triggering trace of operation of said operation circuit upon detection of a predetermined condition within said operation circuit;

a reference clock input for receiving a reference clock signal;

a clock circuit connected to said function clock circuit for receiving said function clock signal and to said reference clock input for receiving said reference clock signal, said clock circuit generating an oscillator clock signal synchronous with one of said function clock circuit and said reference clock signal;

a trace first-in-first-out buffer having an input connected to said function clock circuit and said operation circuit for storing trace data in synchronism with said function clock signal and an output connected to said phase locked loop clock circuit for outputting trace data in synchronism with said oscillator clock signal; and

a trace output port connected to said output of said trace first-in-first-out buffer outputting trace data from said target device; and

an emulator connected to said trace output port for sensing said trace data in synchronism with said oscillator clock signal.

2. The debug and emulation system of claim 1, wherein:

said emulator includes

a reference clock generator connected to said reference clock input for generating said reference clock signal; and

a clock control circuit connected to said clock circuit of said target device for controlling whether said oscillator clock signal is synchronous with said function clock circuit or with said reference clock signal.